We claim:

1. A method to initialize information disposed in an information storage and retrieval system comprising a data cache and one or more information storage media comprising a plurality of addresses, comprising the steps of:

receiving an initialization command, wherein said initialization command comprises a range of addresses, wherein said plurality of addresses includes said range of addresses;

forming and saving state information;

generating and saving a plurality of indicators, wherein each of said plurality of indicators has a first value and a second value;

setting each indicator in said plurality of indicator to said first value;

providing an ending status signal;

wherein said receiving step, said forming step, said generating step, said setting step, and said providing step are performed substantially synchronously.

2. The method of claim 1, wherein said information storage and retrieval system is capable of communicating with a host computer, further comprising the steps of:

issuing said initialization command by said host;

detecting said ending status signal by said host computer; and

disconnecting by said host computer from said information storage and retrieval system;

wherein said issuing step, said receiving step, said forming step, said generating step, said setting step, said providing step, said detecting step, and said disconnecting step, are performed substantially synchronously.

3. The method of claim 1, wherein said plurality of indicators comprises a bitmap comprising a plurality of bits, wherein said plurality of bits includes a bit for each address comprising said range of addresses.

4. The method of claim 3, wherein said initialization command comprises an erasure command.

5. The method of claim 4, wherein said erasure command includes an erasure pattern.

6. The method of claim 5, wherein said state information includes said erasure pattern.

7. The method of claim 1, wherein said range of address comprises a range of tracks, further comprising the steps of:

providing an initialization pattern;

initializing the cache image for a first one of said range of tracks to comprise said initialization pattern;

destaging said first track;

setting the indicator for said first track to said second value;

determining if all indicators have been set to said second value;

operative if all indicators have been set to said second value, removing said state information.

8. The method of claim 1, wherein said range of address comprises a range of tracks, further comprising the steps of:

providing an initialization pattern;

receiving from a host computer a READ command for a designated track;

examining said indicators to determine if an indicator for said designated track is set to said first value;

operative if an indicator for said designated track is set to said first value, initializing the cache image for said designated track to comprise said initialization pattern for each portion of said designated track not already in said cache;

reading said designated track from the cache.

9. An article of manufacture comprising a computer useable medium having computer readable program code disposed therein to initialize information disposed in an information storage and retrieval system comprising a data cache and one or more information storage media comprising a plurality of addresses, the computer readable program code comprising a series of computer readable program steps to effect:

receiving an initialization command, wherein said initialization command comprises a range of addresses, wherein said plurality of addresses includes said range of addresses;

forming and saving state information;

generating and saving a plurality of indicators;

setting each indicator in said plurality of indicator to indicate special handling;

providing an ending status signal;

wherein said receiving step, said forming step, said generating step, said setting step, and said providing step are performed substantially synchronously.

10. The article of manufacture of claim 9, wherein said information storage and retrieval system is capable of communicating with a host computer, said computer readable program code further comprising a series of computer readable program steps to effect:

receiving said initialization command from said host computer;

providing said ending status signal to said host computer.

11. The article of manufacture of claim 9, wherein said plurality of indicators comprises a bitmap comprising a plurality of bits, wherein said plurality of bits includes a bit for each track comprising said range of addresses.

12. The article of manufacture of claim 11, wherein said initialization command comprises an erasure command.

13. The article of manufacture of claim 12, wherein said erasure command includes an erasure pattern.

14. The article of manufacture of claim 9, wherein said range of address comprises a range of tracks, said computer readable program code further comprising a series of computer readable program steps to effect:

obtaining an initialization pattern;

initializing the cache image for a first one of said range of tracks to comprise said initialization pattern;

destaging said first data track;

setting the indicator for said first data track to said second value;

determining if all indicators have been set to said second value;

operative if all indicators have been set to said second value, removing said state information.

15. The article of manufacture of claim 9, wherein said range of address comprises a range of tracks, said computer readable program code further comprising a series of computer readable program steps to effect:

obtaining an initialization pattern;

receiving from a host computer a READ command for a designated track;

examining said indicators to determine if an indicator for said designated track is set to said first value;

operative if an indicator for said designated track is set to said first value, initializing the cache image for said designated track to comprise said initialization pattern for each portion of said designated track not already in said cache;

reading said designated track from the cache.

16. A computer program product usable with a programmable computer processor having computer readable program code embodied therein to erase information disposed in an information storage and retrieval system comprising a data cache and one or more information storage media comprising a plurality of addresses, comprising:

computer readable program code which causes said programmable computer processor to receive an initialization command, wherein said initialization command

comprises a range of addresses and an initialization pattern, wherein said plurality of addresses includes said range of addresses;

computer readable program code which causes said programmable computer processor to form and save state information, wherein said state information comprises said initialization pattern;

computer readable program code which causes said programmable computer processor to generate and save a plurality of indicators, wherein said plurality of indicators includes an indicator for each track comprising said range of addresses;

computer readable program code which causes said programmable computer processor to set each indicator in said plurality of indicators to indicate special handling;

computer readable program code which causes said programmable computer processor to provide an ending status signal;

wherein said receiving step, said forming step, said generating step, said setting step, and said providing step are performed substantially synchronously.

17. The computer program product of claim 16, wherein said information storage and retrieval system is capable of communicating with a host computer, further comprising:

computer readable program code which causes said programmable computer processor to receive said initialization command from said host computer;

computer readable program code which causes said programmable computer processor to provide said ending status signal to said host computer.

18. The computer program product of claim 16, wherein said initialization command comprises an erasure command and an erasure pattern.

19. The computer program product of claim 16, wherein said range of address comprises a range of tracks, further comprising:

computer readable program code which causes said programmable computer processor to obtain an initialization pattern;

computer readable program code which causes said programmable computer processor to initialize the cache image for a first one of said range of tracks to comprise said initialization pattern;

computer readable program code which causes said programmable computer processor to destage said first data track;

computer readable program code which causes said programmable computer processor to set the indicator for said first data track to said second value;

computer readable program code which causes said programmable computer processor to determine if all indicators have been set to said second value;

computer readable program code which, if all indicators have been set to said second value, causes said programmable computer processor to remove said state information.

20. The computer program product of claim 16, wherein said range of address comprises a range of tracks, further comprising:

computer readable program code which causes said programmable computer processor to obtain an initialization pattern;

computer readable program code which causes said programmable computer processor to receive from a host computer a READ command for a designated track;

computer readable program code which causes said programmable computer processor to examine said indicators to determine if an indicator for said designated track is set to said first value;

computer readable program code which, if an indicator for said designated track is set to said first value, causes said programmable computer processor to initialize the cache image for said designated track to comprise said initialization pattern for each portion of said designated track not already in said cache;

computer readable program code which causes said programmable computer processor to read said designated track from the cache.